IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Brian C. Barnes, et al	Group Art Unit:	2137
Serial No.:	10/010,161	Examiner:	Ali Abyaneh
Filed:	11/13/01	Atty. Dkt. No.:	2000.056700
For:	Memory Management System And Method Providing Linear Address Based Memory Access Security	Client Docket:	TT4087

REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit this Reply Brief to the board of Patent Appeals and Interferences in response to the Examiner's Answer dated June 29, 2006. The statutory response due is two months from the date of the Examiner's Answer, therefore, it is due August 29, 2006. Since this Reply Brief is being filed on or before August 29, 2006, it is timely filed.

It is believed that no fee is due for the filing of this Reply Brief. However, should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to the enclosed material, or should an overpayment be included herein, the Commissioner is authorized to deduct or credit said fees from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.056700.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also

constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

ARGUMENT

In the Answer, the Examiner repeated the rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103 set forth in the final rejection in this application. It is believed that the reasons that those rejections are improper are expressly set forth in the Appeal Brief filed in this matter. In particular, the Applicants respectfully submit that the Examiner erred in rejecting that claims 1-37. Therefore, Applicants respectfully request that the rejection of claims 1-9, 11-13, 23, 32, and 36-37 under the 35 U.S.C. §102(b), and claims 10, 20, 22, 26, and 35 under 35 U.S.C. § 103(a) be reversed.

With regard to rejection of claim 1, the Examiner's Answer, at page 9, alleges that because ***Maruyama*** teaches a processor 340 is connected through a bus 15 to a memory unit 10, the memory unit 10 includes a DRAM 19 and a Master ID Table 24 (see column 5, lines 7-11), it discloses use of a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory, as set forth in claim 1. The Examiner further asserts that ***Maruyama*** also discloses using a linear address and accessing at least one security attribute data structure (Master ID Table 24) located in a memory (memory unit 10) to obtain a security attribute of a selected memory page in the memory (see column 5, lines 20-40), since it describes use of the Master ID Table 24 and the memory unit 10. In particular, at page 10, in the Answer, the Examiner asserts since ***Maruyama*** discloses that the memory unit 10 includes "all of the component in fig. 4 except for the system bus 15, bus adapter 320, processor 330, 340 and low speed bus 13" (column 5, lines 7-11), in ***Maruyama*** the Master ID Table 24 and the DRAM 19 are within and part of the memory unit 10. The Examiner concludes that since Applicants purportedly acknowledge that DRAM 19 includes the accessed memory pages and ***Maruyama*** teaches that the memory unit 10 among the other components

includes a DRAM 19 and a Master ID Table 24, therefore, the memory unit 10 includes the Master ID Table 24 and the selected memory pages being included in the DRAM 19 (see fig.4 and column 5, lines 7-11).

Maruyama is completely silent regarding using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory. Instead, ***Maruyama*** teaches that unauthorized bus masters should not be permitted to access the dynamic random access memory (DRAM) 19 under certain circumstances. Thus, ***Maruyama*** fails to provide linear address based memory access security.

Claim 1 of the present invention describes and claims accessing a security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory. However, ***Maruyama*** hosts the bus master identification table 24 in a different memory than the accessed memory pages. ***Maruyama*** does not disclose use of a common memory for the two as set forth above; it is merely directed to avoiding unintended modifying of a certain portion of the memory, which may be accessible to read only. In contrast, claim 1 of the present invention calls for using a linear address to access a security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory. ***Maruyama*** does not describe or suggest the use of the memory that includes the security attribute data structure *and* the selected memory page. Therefore, ***Maruyama*** cannot anticipate use of the linear address to access one or more security attribute data structures located in a memory to obtain a security attribute of the selected memory page in the memory, as called for by claim 1 of the present invention.

Thus, Applicants submit that ***Maruyama*** does not describe or suggest using a linear address to access at least one security attribute data structure located in a memory to obtain a

security attribute of a selected memory page in the memory, *i.e.* the memory that includes the security attribute data structure *and* the selected memory page.

To support his rationale for § 102 rejections, however, the Examiner instead states that ***Maruyama*** teaches the Master ID Table 24 located on the memory unit 10. Furthermore, at page 9 of the Answer, the Examiner asserts that ***Maruyama*** also discloses using a linear address and accessing at least one security attribute data structure (Master 10 Table 24) located in a memory (memory unit 10) to obtain a security attribute of a selected memory page in the memory. See col. 5, lines 20-40. Thus, according to the Examiner, since the master ID table 24 is located on the memory unit 10 and a linear address is purportedly used for accessing a security attribute data structure, both the Master ID Table 24 and the linear address are described to be hosted on a same memory unit. In other words, the Examiner alleges that since the bus Master ID Table 24 is located in the same memory as the accessed memory pages (according to the Examiner), a lookup table is accessed on the same memory unit. Applicants respectfully disagree.

Maruyama describes hosting the bus master identification table 24 in a EEPROM or a battery back-up RAM, and does not teach that the bus master identification table 24 should be hosted on the DRAM 19 that includes the accessed memory pages. See ***Maruyama***, col. 5, ll. 33-38 and Figure 1. Thus, Applicants submit that ***Maruyama*** does not describe or suggest using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory, *i.e.* the memory that includes the security attribute data structure *and* the selected memory page.

Accordingly, Applicants respectfully submit that claims 1-9, 11-13, 23, 32 and 36-37 are allowable over the prior art of record for at least the reasons set forth in the Appeal Brief filed in

this matter. Furthermore, Applicants note that claims10, 20, 22, 26 and 35 are in condition for allowance as well for at least the aforementioned reasons.

In view of the foregoing, it is respectfully submitted that the Examiner erred in rejecting the claims pending in the present application. Accordingly, Applicants respectfully request that the Board overrule the Examiner's decision and issue instructions that all pending claims be allowed.

In light of the arguments presented above, Applicants respectfully assert that all of the claims are allowable. Accordingly, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned at the Houston, Texas telephone number (713) 934-4089 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Date: August 25, 2006

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BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATES PATENT AND TRADEMARK OFFICE

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